REMARKS

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 are pending in this application.

Claim 36 has been amended as the "amendment to the claims filed on 06/05/03 does not comply with the requirements of 37 CFR 1.121(c) because in claim 36 . . . the limitation of 'a conductive layer provided over a semiconductor substrate" in line 2; and the limitation of "said conductive layer" in line 4 should be shown in brackets for deleted matter." (Office Action at 2). Applicant has rewritten claim 36 so that the deleted limitations are shown in brackets, in compliance with 37 CFR 1.121(c).

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 stand rejected under 35 U.S.C. § 102 as being anticipated by Agarwal et al. (U.S. Patent No. 6,297,527) ("Agarwal"). This rejection is respectfully traversed.

The claimed invention relates to an electropolished patterned metal layer formed as part of a semiconductor device. As such, independent claim 29 recites "an insulating layer provided over said substrate" and "an electropolished patterned metal layer provided over said insulating layer, wherein said electropolished metal layer has a thickness of approximately 50 to 300 Angstroms." Independent claim 29 also recites that "a top surface of said electropolished metal layer is electropolished down to said insulating layer."

Independent claim 36 recites a "memory cell" comprising *inter alia* "an electropolished patterned metal layer provided over a substrate, said electropolished metal layer having a thickness of approximately 50 to 300 Angstroms" and "a container capacitor including a lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode." Independent claim 44 recites a "processor-based system" comprising *inter alia* "a container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms."

Independent claim 55 recites a "container capacitor" comprising inter alia "a lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending upwardly therefrom" and "an insulating layer provided over said electropolished patterned metal layer." Independent claim 59 recites a "container capacitor" comprising *inter alia* "a barrier conductive layer," "a lower electrode . . . comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom, said lower electrode having a thickness of approximately 100 Angstroms" and "a dielectric material provided over said electropolished patterned metal layer." Independent claim 60 recites a "container capacitor structure" comprising "an insulating layer provided over a substrate; a plurality of openings provided in said insulating layer; and a plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers."

Agarwal relates to a "high dielectric constant capacitor having a multilayer lower electrode comprising at least two layers--a platinum layer and a platinum-rhodium layer--for use in a random access memory (RAM) cell." (Abstract). According to Agarwal, "[t]he platinum layer of the lower electrode adjoins the capacitor dielectric, which is a ferroelectric or high dielectric constant dielectric such as BST, PZT, SBT or tantalum pentoxide." (Abstract). Agarwal also teaches that "[t]he platinum-rhodium layer serves as an oxidation barrier and may also act as an adhesion layer for preventing separation of the lower electrode from the substrate, thereby improving capacitor performance." (Abstract).

Agarwal does not disclose, teach or suggest the subject matter of claims 29-32, 34-39, 41, 44-47, 49 and 51-64. Agarwal does not disclose "an electropolished patterned metal layer" or "electropolished patterned metal layers," much less "an electropolished patterned metal layer" or "electropolished patterned metal layers" as part of capacitor structures, as in the claimed invention. Applicant notes that the limitation "electropolished patterned metal layer" is simply not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics. The term "electropolished patterned"

describes the physical characteristics of the metal layer in independent claims 29, 36, 44, 55, 59 and 60. Specifically, the term "electropolished patterned" is a limitation of the metal layer. Claim limitations which confer distinct and defined characteristics of a structure have been analyzed by the Federal Circuit in Hazani v. U.S. Int'l Trade Comm'n, for example. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997). In Hazani, the Federal Circuit specifically emphasized that the claims in question, which were directed to a memory cell comprising a conductive plate having a surface that was "chemically engraved," were "pure product claims" and not product-by-process claims. In arriving at this conclusion, the Federal Circuit reasoned that "Hazani argues that the 'chemically engraved' claims are product-by-process claims. We agree with the respondents, however, that those claims are best characterized as pure product claims, since the 'chemically engraved' limitation, read in context, describes the product more by its structure than by the process used to obtain it." Id. Accordingly, in view of Hazani, the limitation "electropolished patterned metal layer" of independent claims 29, 36, 44, 55, 59 and 60 is a structural limitation and not a product-by-process limitation. An "electropolished patterned metal layer," like the "chemically engraved" plate of Hazani, is a *resulting structure* having distinct and defined characteristics and not a product formed by a particular process.

Claims 29-32, 34-39, 41, 44-47, 49 and 51-64 stand rejected under 35 U.S.C. § 102 as being anticipated by Xing et al. (U.S. Patent No. 6,090,697) ("Xing"). This rejection is respectfully traversed.

Xing relates to a "high-selectivity via etching process" that "includes the steps of: forming an etchstop layer 840 of a material selected from the group consisting of Ti--Al, Ti--Al--N, Ta--Al, Al--N, Ti--Al/Ti--N, Ti--Al--N/Ti--N, Ta--Al/Ti--N, and Ti--Al/Ti--Al--N; forming a dielectric layer over the etchstop layer; and etching the dielectric layer with a fluorine-bearing etchant." (Abstract).

Xing fails to disclose the subject matter of claims 29-32, 34-39, 41, 44-47, 49 and 51-64. Xing does not disclose "an electropolished patterned metal layer" or

"electropolished patterned metal layers," much less "an electropolished patterned metal layer" or "electropolished patterned metal layers" as part of capacitor structures, as in the claimed invention. As noted above, the limitation "electropolished patterned metal layer" of independent claims 29, 36, 44, 55, 59 and 60 is not a product-by-process limitation, but rather a *resulting structure* having distinct and defined characteristics. For at least these reasons, Xing fails to anticipate the claimed invention and withdrawal of the rejection of claims 29-32, 34-39, 41, 44-47, 49 and 51-64 is respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By_____

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